White Paper

IMXPWSWP/D
Rev. 1, 02/2004

i.MX Applications Processor
Creating Performance with Stamina for Wireless Communications

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Creating Performance with Stamina for Wireless Communications

Executive Briefing

As we all take our first steps into a brave new world of third generation mobile services, we are participating in a revolutionary new way of conducting business, where mobility no longer limits our productivity. We are no longer tethered to a power outlet or confined to a few square feet of office space. We see ourselves as having all the power and sophistication of a hard-wired home or office right in the palms of our hands. However, we also know that mobile systems have an Achilles heel—a mobile power source. No matter how powerful our mobile systems become, the amount of work performed is always limited by the life of the battery. That is why low power consumption must be as important a design consideration in mobile communications devices as speed and ability, resulting in what we call performance with stamina.

Now that we are entering a new realm of 3G deployment, carrying broadband access around in our pockets, wireless communication access and processing capabilities are increasing dramatically, and the drain on battery life is increasing right along with them.

Long battery life is important because a business day is not a sprint. It's a marathon of communication. High performance smartphones and wireless PDAs should not be accompanied with a pocketful of batteries. Future generations of wireless hand held communication devices must strike a high level balance between performance and stamina (long battery life), which is a particular strength of Motorola's i.MX family of application processors based on ARM™ technology.

The i.MX family of embedded application processors offers a leap in performance and integration from earlier DragonBall™ processor products. The i.MX family helps cut the time it takes to perform the tasks required while at the same time helps to extend the time you have to get more work done. To achieve this difficult combination, i.MX products are being developed with two overriding priorities:

Performance—The ability to support a broad range of demanding applications in a mobile environment.

Stamina—Increased battery life means more production, more entertainment, and the satisfaction that you are getting the most out of new technology.

ARM POWERED®

The i.MX family of application processors based on ARM technology is designed for smartphone technology, wireless PDAs, and other mobile wireless applications. With the rapid advent of new and powerful wireless services for very small, hand held devices—broadband Internet access, video capture, live video streaming, etc.—it's imperative that we offer our users the hardware and software that can quickly process these new services. It is also our responsibility to push the limits of power management, because, as will be explained later in this paper, battery technology will never catch up to us and can't bail us out of this dilemma.

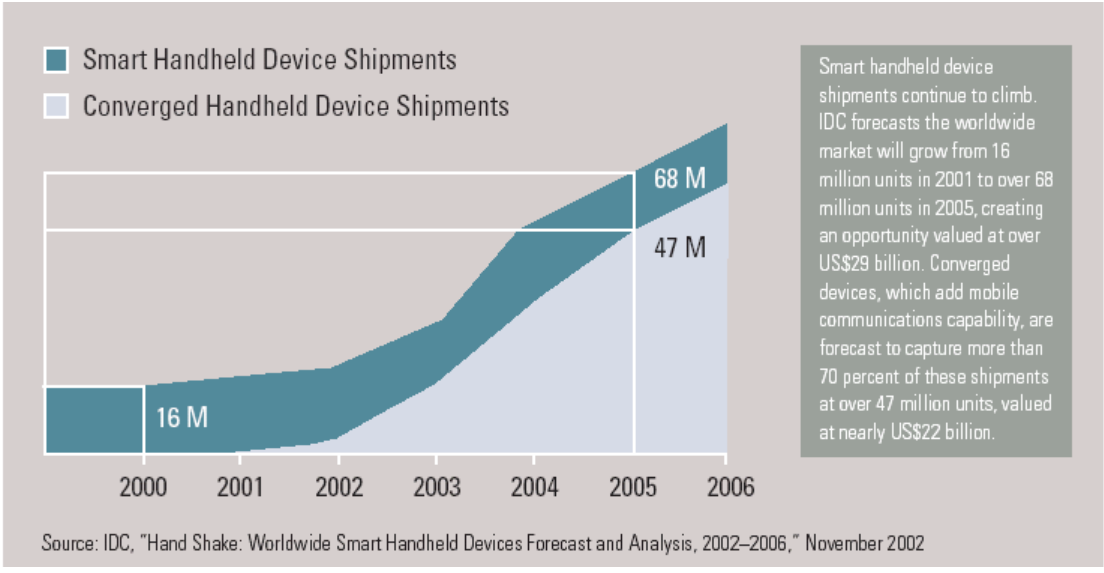
What differentiates the i.MX is its level of feature integration around an industry standard ARM core processor. The first member of the i.MX family, the i.MX1, is an ideal combination of price, performance, and low power consumption. It is engineered with the power and stamina expected to handle the ever more complex system requirements of the newest handheld devices, delivering fast access for long periods of time.

Future generations of the i.MX family will incorporate advanced floating-point technology in hardware. Floating point is designed to not only boost the performance of such advanced features as MPEG4 and 3-D graphics, it is engineered to refine the appearance of all graphic displays, including the appearance of text fonts.

We already know that as processor performance goes up, battery life goes down, so we have to use more efficient software and sophisticated semiconductor process technology to give our DragonBall application processor products more stamina, to close the gap between performance and battery life. Such design techniques as selective hardware acceleration, dynamic frequency control, direct memory access channels, and clock gating all add to the overall efficiency of i.MX, providing more work from less energy.

Motorola's architectural license allows us to make architectural enhancements to the ARM core. However, we have chosen not to add any proprietary modifications in order to help ensure that customers maintain software compatibility between ARM architectures and the ability to use standard development tools. Instead, we work very closely with ARM Ltd. to help make their processor a more efficient core for our i.MX application processor. This means that customers who purchase the i.MX know they have at its heart a processor that is engineered to be 100% compatible with the industry standard ARM instruction set and architecture, and that they don't have to worry about code compatibility.

Motorola has built three development platforms for the development of wireless handheld and smartphone products—the Innovative Convergence™ platforms for 2.5G and 3G cellular and a CPU Platform for handheld computing devices, such as PDAs. No other total system is as highly integrated, cost effective, and power efficient as the Motorola platforms, which are continually improved to support new technologies and new services as they reach the market.

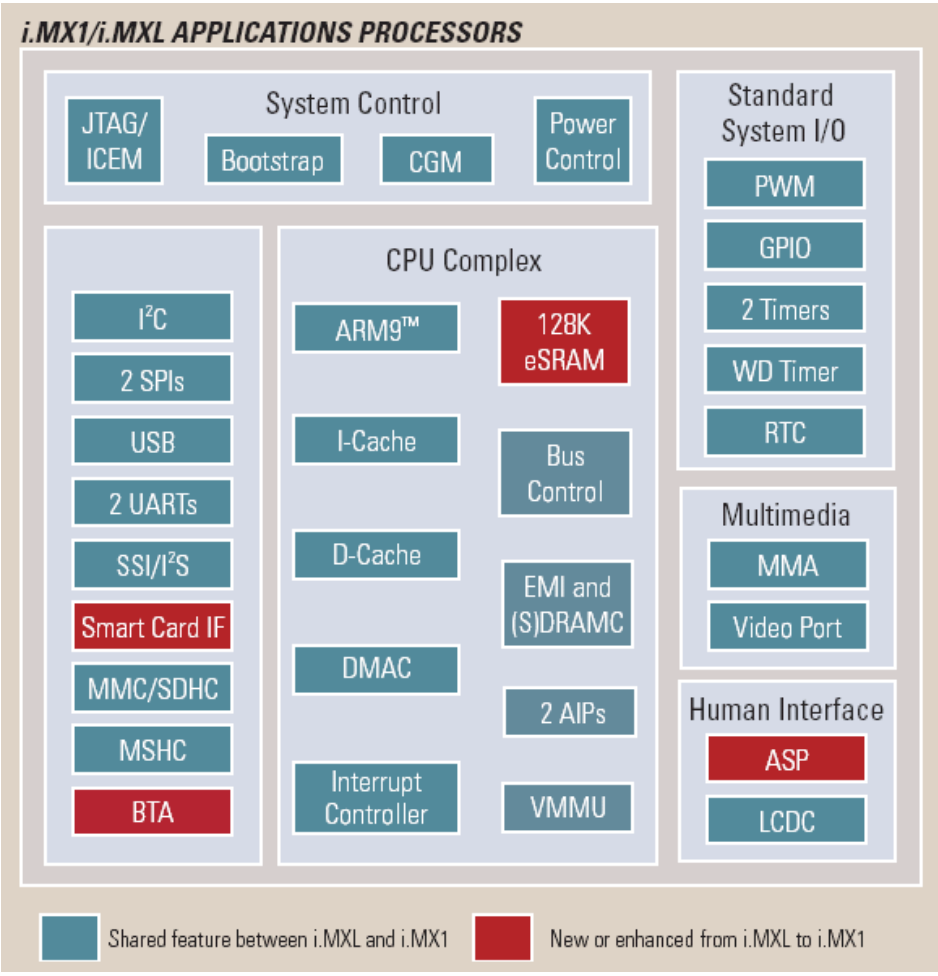


The Processor

Establishing a new processor architecture and bringing it to market is very expensive. It involves not only the time and expenses associated with design and development, but also a significant investment in tools, collateral material, promotional programs, and an attractive licensing system to encourage new adopters. ARM Ltd. has already done all this, and very successfully. ARM processors have gained industry wide acceptance and have several established advantages to offer, including: upward migratable software compatibility; an extensive portfolio of cores; a high performance roadmap for future products; and a network of multiple providers of ARM processor products.

Choosing the ARM processor core for i.MX products makes sound financial sense and allows us to use our resources to develop key peripherals that distinguish i.MX from its competitors and make it the most efficient processor for wireless handheld communication devices in the industry.

Motorola has had a long and successful alliance with ARM Ltd, and we are now a leading supplier of devices that are based on the ARM architecture. As an architectural licensee we also work with ARM Ltd. on the definition of key IP (Intellectual Property) blocks. With our experience in high-end PowerPC™ systems, Motorola has the knowledge and the skills to assist ARM Ltd. in creating the additional blocks required to support high performance systems. For instance, we helped to create the L2 cache controller for the ARM11 core.



With ARM core technology, i.MX is the next generation DragonBall processor that offers considerable higher levels of performance and integration than earlier DragonBall processor products. The first member of the family, the i.MX1, includes features such as:

- The ARM920T™ core, which combines an ARM9TDMI processor core with a 16Kbyte instruction cache and a 16Kbyte data cache.
- Color LCD controller.
- 128 Kbyte embedded SRAM to decrease external memory access and increase system performance.
- Video port which supports glueless interface to external CMOS sensor video data input.
- Analog Signal Processor module with A/D converter for touch panel control.
- Bluetooth™ accelerator, which, together with a software stack, external RF IC, and very few discretes implements a Bluetooth node.

However, there is more to the i.MX than a list of features and capabilities. The processes used in designing and building a powerful applications processor go a long way toward determining whether it will be strong enough to power the new “always on” portable appliances reaching the market, yet economical enough to be, well, “always on.”

Motorola has a great deal of experience in wireless communications—over seventy years building wireless products, and fifty years in the semiconductor industry. We are uniquely qualified to start with a high performance processor core and build a high level of integration and system optimization around that core. Doing so provides the features needed to process the latest wireless services cost effectively with low power consumption. We learned a long time ago that low power is just as important as high performance when designing and building portable communications devices. Because high performance usually requires high power and low power sacrifices at least some performance, the trick is to find the perfect balance between the two within a particular design. We optimize for performance when speed is an absolute must and build everything else for low power. There are a number of design and manufacturing strategies for achieving economical performance, and Motorola is adept at implementing these practices, at system-level, chip-level, and even transistor-level designs, to achieve performance with stamina.

Dual V_T—Each transistor in a semiconductor design has an associated threshold voltage (V_T) that determines at what voltage level the gate is triggered to open or close. Typically, a lower V_T transistor offers higher performance because the voltage doesn’t have to swing as far to trigger the gate. However, the manufacturing techniques necessary to produce low V_T transistors tend to make them higher leakage devices, so the standby current drain is higher than what you want to include in a portable, battery powered product. In the past, we had to make a choice whether we wanted to tune a device for high speed, in which case we would have poor standby current, or design it using higher V_T transistors which would not run as fast but would have less standby current drain. Now we have the ability to include both high and low V_T transistors in the same chip, using only low V_T transistors for those critical path circuits required to get the speed that we want. The bulk of the device can then use the higher V_T transistors, which have the advantage of lower standby current.

Well-biasing—Essentially, standby current drain is electrons “leaking” through a gate junction of thin oxide within the transistor. The amount of current flow is a function of the voltage across the junction. The greater the difference between voltages on both sides of the junction, the greater the leakage—more current is being drained, even in standby mode. By biasing up the substrate voltage to more closely match the voltage on the other side of the transistor, the voltage across the junction is lowered, thus reducing the leakage. This is well-biasing, and it helps reduce current drain on a transistor level whereas Dual V_T is a chip-level technique. Both methods can be used in a single device to minimize standby current drain.

Dynamic Voltage Frequency Scaling (DVFS)—This is simply adjusting the clock speed and power supply on the fly to lower current drain when full speed operation is not required. For instance, there is no reason to run a clock at 200 MHz if the application only requires 50 MHz. Slowing the clock means the operating voltage can be lowered, which, in turn, lessens the demand for battery power.

Dynamic Memory Access (DMA)—This facilitates data movement with minimal processor intervention. DMA is engineered to allow pathways between peripherals and memory to bypass the processor. It increases efficiency and performance because of short and direct data paths, and it is designed to save the processor from allocating power and performance to this particular task. This means the CPU can either be used to perform other functions, which increases system performance, or, since it has less work to do, it can be slowed down to save power.

Clock Gating—This is an effective strategy for reducing power consumption while maintaining the same levels of performance and functionality. Basically, a circuit uses power when it is being clocked, but leaks a smaller amount of current (measured in micro-amps) when its clock has been gated, or tuned off. By shutting off the clocks of unused portions of the i.MX, we have realized significant power savings during operation. The i.MX cycles are engineered to clock on an off at the individual instruction level, and not only in the ARM core but in the peripherals as well.

Partitioning—Many tasks in an embedded system can be implemented in either dedicated hardware or in software on a programmable core. Generally, software is more flexible and cheaper, but hardware is faster and consumes less current. The challenge is partitioning tasks between hardware and software to take best advantage of their attributes to get the fastest yet most efficient solution. A better model for speed and efficiency can be realized by committing intensive machine cycling tasks to hardware accelerators rather than software. However, this must be accomplished in a manner that preserves the flexibility of software where that flexibility is most important.

For instance, stable, computer intensive functions that are required in key applications can be built in hardware to get the performance edge when flexibility is not the major issue. Functions that are less well-defined and can change frequently, (such as Digital Rights Management where there is no universal standard), the value of software flexibility may outweigh the benefits of dedicated hardware. Intelligent hardware/software partitioning decisions of this sort accomplish a great deal toward high performance, low power results.

It’s Not About the Megahertz

High megahertz processors on a very wide, very fast bus can afford to run flat-out, pushing data unencumbered down the pipe. However, in portable wireless systems, buses tend to be much slower and narrower and can only carry so much data at a time. When you increase the CPU clock you need to feed it with data and instructions. As this data is pushed through the bus and hits a bottleneck, say, trying to read and write to the external main memory, an over-clocked processor will just burn up excess energy with the extra megahertz and subsequently drain the battery. This can be somewhat mitigated by employing L2 (Level 2) cache in the system, which stores the most critical and often-used information in SRAM very close to the processor. Future i.MX offerings are expected to employ L2 cache, which reduces the number of times the CPU has to hit the external memory bottleneck, but that alone doesn’t address the limitations of the entire system bus.

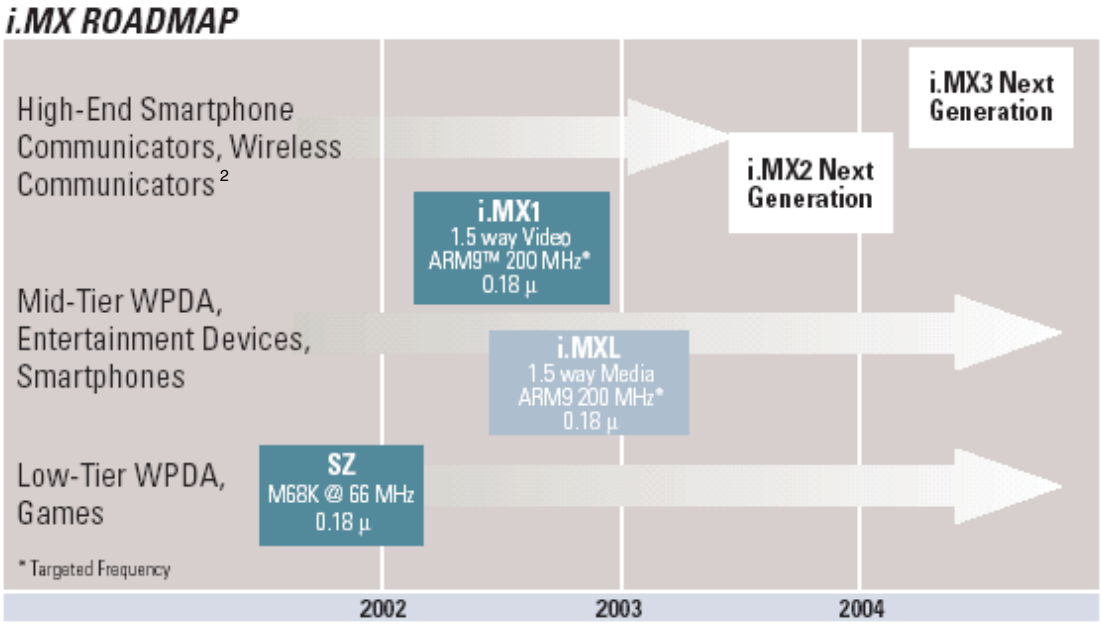
We have significant experience managing system buses to get the most out of our processors—to get the optimum balance of performance and power consumption. Our CPU Platform based on the ARM926 core (used in our second generation i.MX solutions) is designed with a multi-master crossbar switch is engineered to allow us multiple masters (including the CPU) to talk with multiple slaves (peripherals) simultaneously. This type of switch design has been used for some time in large high-speed data networks, but now we have successfully transferred this technology to the portable wireless environment. The crossbar switch allows us to maximize the system level performance by keeping all the engines fed with data and instructions so there is little “dead time” and less “waiting” for another data transfer to complete.

Improved performance is not about just cranking up the clock and getting more megahertz through the CPU, it’s about using the megahertz you have to get more work from the entire system without wasting any time or energy in the process. This will become more critical as we move from GSM (Global System

for Mobile communications) to far more sophisticated and feature rich technologies, such as General Packet Radio System (GPRS), Enhanced Data for GSM Evolution (EDGE), and Universal Mobile Telecommunications Service (UMTS). Smartphones and PDAs are expected to employ combinations of services, that are also expected to include Bluetooth and 802.11 WLAN capabilities, and all these are expected to require increasingly more powerful and efficient processors.

For smartphones, low power consumption is as important a design consideration in mobile communications devices as speed and features. Design engineers know that real-world performance is not accurately measured by clock frequency. Over clocking the processor does nothing to mitigate a slow memory system. The i.MX family is engineered to do the same work quickly at low clock speeds and low clock speeds translates into critical power savings. This winning combination is the model for i.MX, now and in the future.

Power performance such as this means that an i.MXL processor PDA is engineered to enable more than six hours movie play time using a 1000mAH battery, and can offer a standby time of between 50 and 70 days. To consumers, this is the equivalent of watching a feature film twice over on an i.MXL processor PDA, or going on a "round the world" business trip and returning—without ever charging the PDA device. The new i.MX21 offers CIF 30 fps video encode and decode, sending a secure transaction while playing an MP3 or videoconferencing at 15 fps with a 35 percent to 65 percent reduction in power consumption.[1]



Closing the Gap

Battery life, or stamina, in the real world is every bit as important to the wireless user as performance. Ask anyone who's lost a connection because his or her mobile phone has run out of energy. Unfortunately, advances in processor performance, with their associated appetites for power, are far outstripping advances in battery life. Moore's Law states that processor performance doubles every eighteen months. Meanwhile, battery energy density only doubles *every ten years*. What's more, system performance adheres to another

1. Improvement over i.MX1.
2. Except for historical information, all of the expectations and assumptions, contained in the foregoing are forward-looking statements involving risk and uncertainties. Important factors that could cause actual results to differ materially from such forward-looking statements, include, but are not limited to, the competitive environment for our products, changes of rates of all related services, and legislation that may affect the industry. For additional information regarding these and other risks associated with Company's business refer to the Company's reports with the SEC.

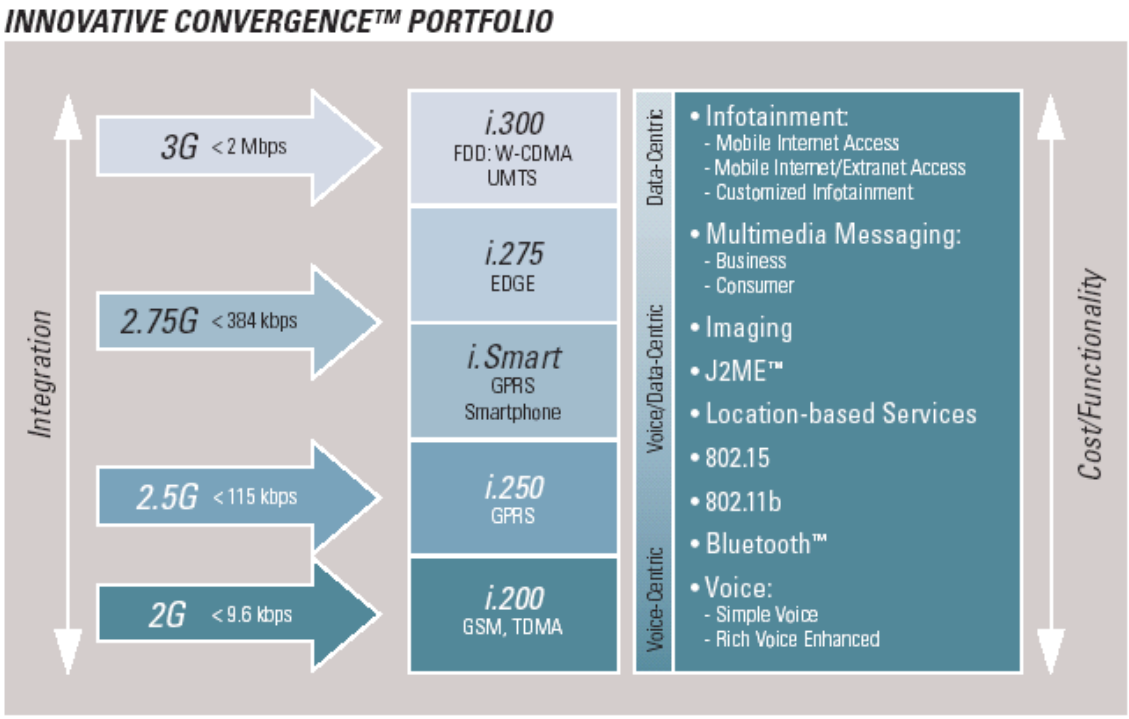
law—Shannon's Law. It shows that communication system performance requirements are doubling every eight-and-a-half months—about twice the rate of processor performance and *over fourteen times the rate of improved battery life*.

This is why we work so hard to save energy in our designs, from transistor-level to system-level. We must continue to push the performance limits, however, we cannot afford to emphasize speed over stamina. We know that battery technology will never keep up with us, so it is up to us to close the gap between system power requirements and the availability of battery power. Expectations are very high. We must offer components and systems that OEMs and ODMs can use to build what consumers are demanding—pocket-sized wireless communicators and business tools that are on whenever they need them.

Think System

It's important to keep in mind that i.MX is part of a larger Motorola wireless application system. The fully integrated Innovative Convergence Platform offers the cutting edge chipset, software engine, and development environment necessary for 2.5G and 3G cellular development that supports Bluetooth and Java™ 2 Micro Edition (J2ME™) implementation. Smartphone development hinges on successfully combining cellular functionality with application processing in one handset. The platform is designed to integrate the i.MX seamlessly with a companion cellular processor. Using this approach, we can change and enhance the DragonBall processor without requiring the need to re-certify the cellular functionality of the smartphone with the carriers. Motorola has leveraged over twenty years of cellular experience to develop the i.250 platform for GSM/GPRS handsets and the i.300 for GSM/UMTS appliances.

Similarly, we've developed the CPU Platform for handheld computer applications, such as new PDAs with such multimedia features as audio and video playback, as well as imaging capabilities. The Motorola i.MX platforms are multi-OS and real-time-OS ready and include Bluetooth wireless technology-enabled interfaces. Each platform is compact, highly integrated, and very power efficient, having been designed and manufactured using the low-power, yet performance enhancing techniques discussed earlier. In addition, we are among the first companies to offer an application processor with 1.8V I/O, offering an efficient interface with the advanced 1.8V memory products. And we are continually expanding these systems to offer support for new technologies and new services as they emerge in the marketplace—new, advanced display technologies, including smart panels; streaming video; multiple operating systems; and the far-reaching capabilities of the personal server.



Conclusion

As Buyers of pocket-sized wireless devices, now and in the future, we expect a workable, real world balance of performance and stamina. This is particularly applicable in the emerging 3G environment, because we expect to use the more powerful and feature rich 3G products extensively. That's the challenge. Advanced services provide more value to us, but demand more from our batteries. We will not accept frequent disconnection from the network because our batteries keep running low, nor will we forego new services because we don't have adequate performance.

As we have seen, battery technology is struggling to keep up with processing technology and system requirements. It is our charge to close the gap from the top down, meaning getting more work for longer periods of time from whatever the batteries have to offer. In this brief paper we have explored the techniques we use to provide world-class handheld wireless communication solutions to our customers and the reasons why we use these techniques. It goes without saying, however, that these may not be adequate for what's out there beyond 3G, and to reach our goals of performance with stamina in all our future applications, we will be pushing ourselves without rest, and our performance and our stamina will be constantly tested.

NOTES

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